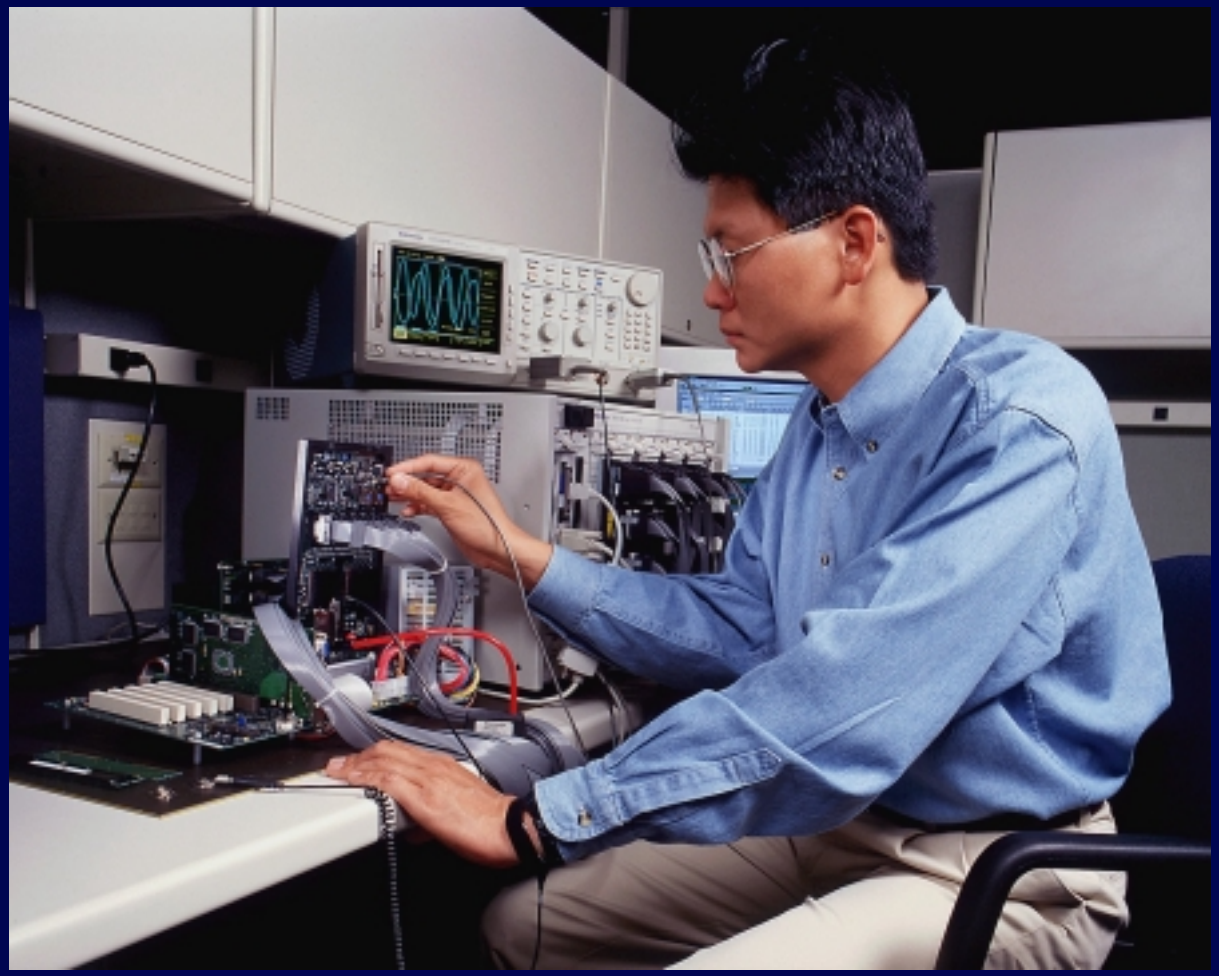
Rambus Protocol Testing



Logic Analyzer Support for Direct Rambus

- What measurement challenges does Rambus present?
- What is so unique about READ data?
- What does the Tektronix solution look like?
- How does it help?
- How do I get it?
- What related solutions does Tektronix offer?

RAMBUS® DEVELOPER

Tektronix®

Logic Analyzer Support for Direct Rambus

- What measurement challenges does Rambus present?
- What is so unique about READ data?
- What does the Tektronix solution look like?
- How does it help?
- How do I get it?
- What related solutions does Tektronix offer?

RAMBUS® DEVELOPER

Tektronix®

Direct Rambus Measurement Challenges

- Debugging and optimizing protocol usage
  - Chipset validation
  - Debugging motherboard & BIOS designs
  - Optimizing memory efficiency
  - Verifying power management operation
- Tracking down signal quality problems
  - Verifying signal quality over a range of functional conditions
  - Identifying signal quality problems that cause isolated failures
- Relating Rambus activity to other system activity
  - System validation
  - Tracking down complex failures

RAMBUS® DEVELOPER

Tektronix®

Key - Functional Trace of Protocol

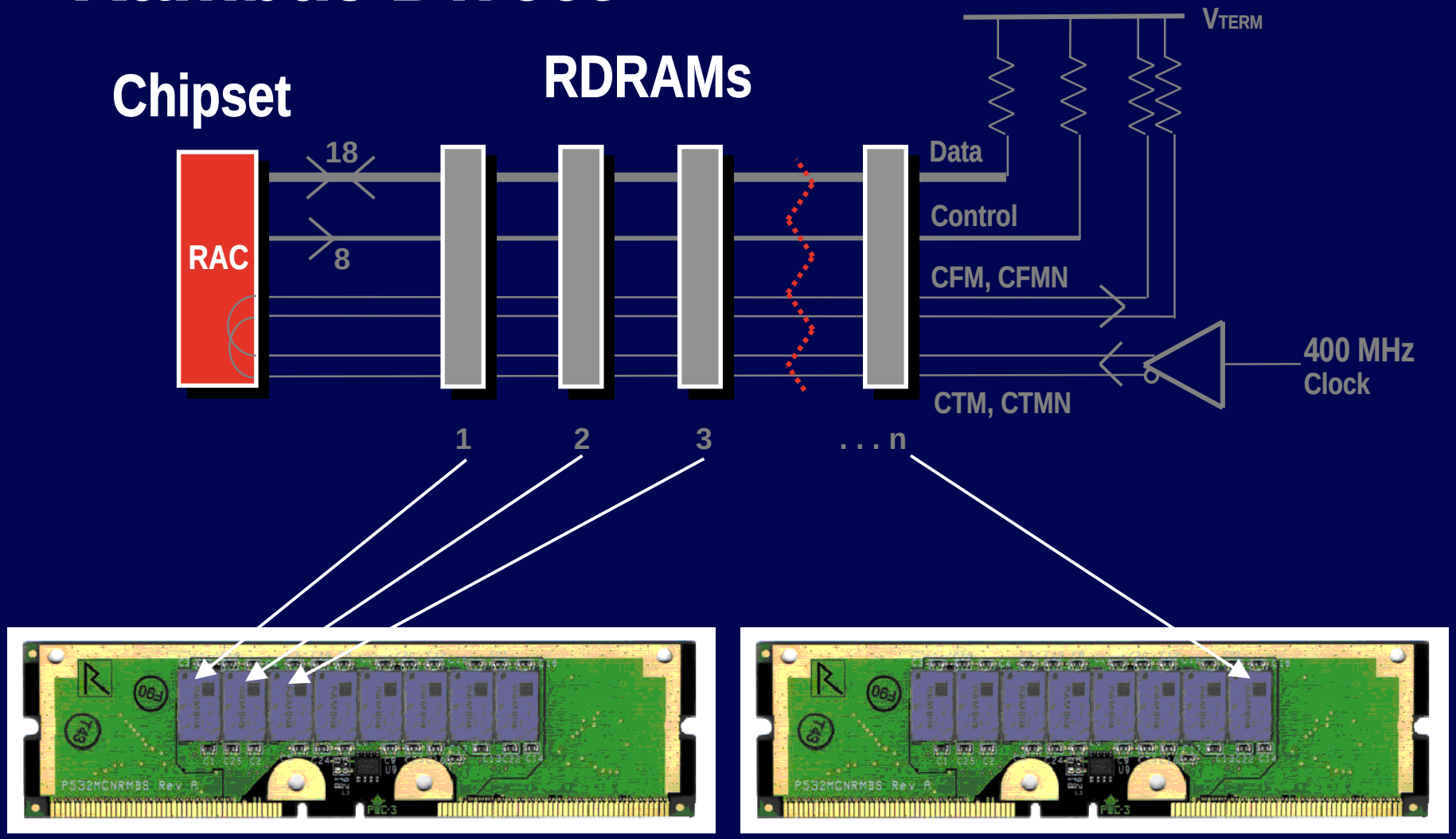
Challenge - Rambus is much faster than other buses

- 800 MHz data rate
  - (400 MHz clock with double-pumped data)
- Data valid window is very short
  - ~400 ps
- Edge rates are very fast
  - ~200 ps
- READ data is not readily visible on the bus
- Signal quality is a primary concern

RAMBUS® DEVELOPER

Tektronix®

Rambus Direct



RAMBUS DEVELOPER

Tektronix

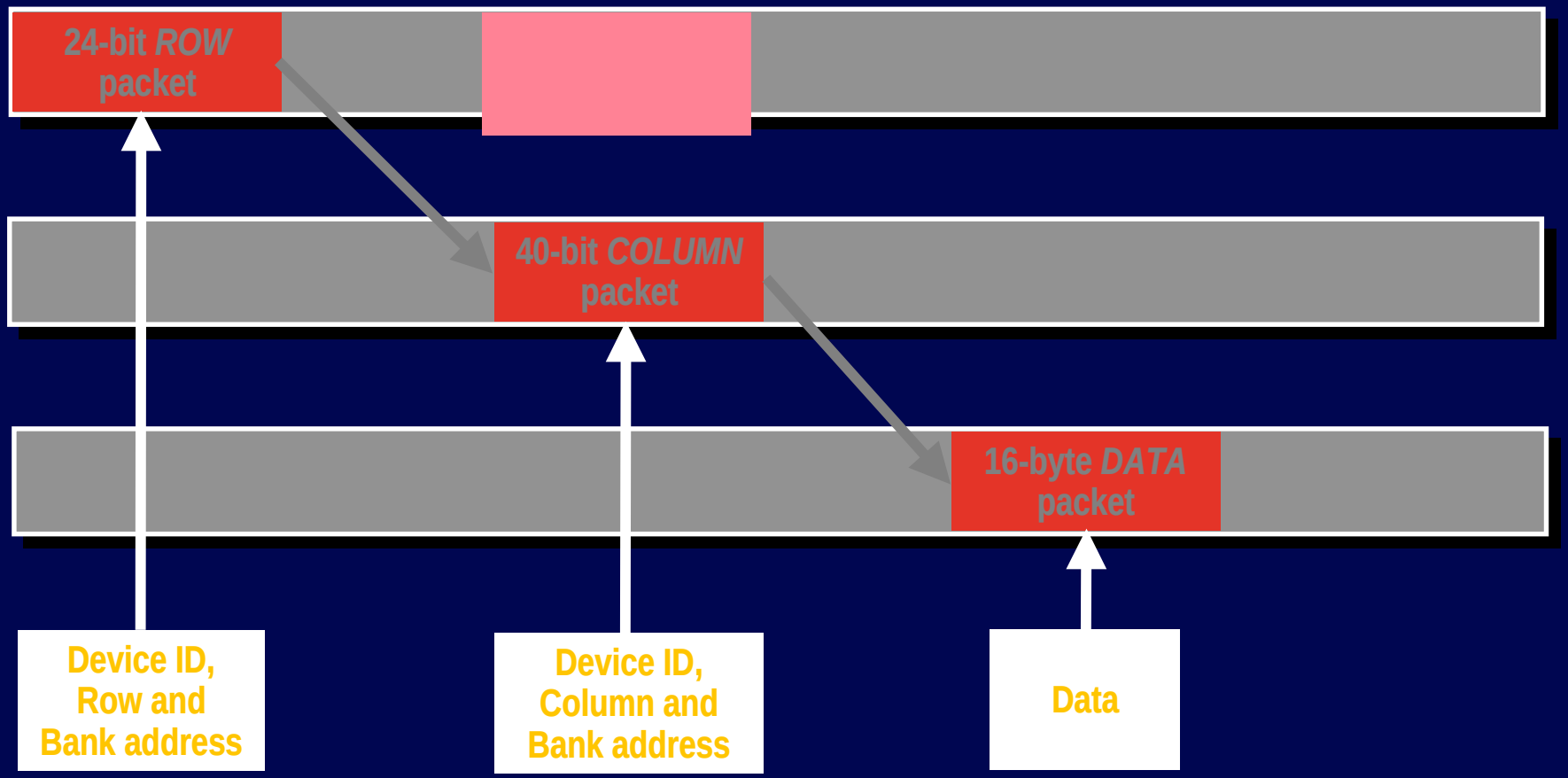
Key - Functional Trace of Protocol

- Challenge - protocol appears convoluted on the physical bus
  - All packets occur in 8-bit deep transfer bursts
    - Row packets (ROWA & ROWR) are 3 bits x 8 (24 bit field)
      - ROWA - Row Activate, ROWR - Row Operation Packets
    - Column packets (COLC, COLM & COLX) are 5 bits x 8 (40 bit field)
      - COLC - operation, COLM - mask, COLX - extended operation packets
    - Data packets are 16-18 bits x 8 (128-144 bit field)
  - Packets are not all aligned on the same clock boundaries
    - Strict alignment is not enforced
    - Packet alignment timing is adjusted to maximize performance
    - Alignment changes dynamically in normal operation
- Effective triggering on protocol is an essential requirement for a useful

RAMBUS DEVELOPER

Tektronix

Rambus Transaction Pipeline



RAMBUS DEVELOPER

Tektronix

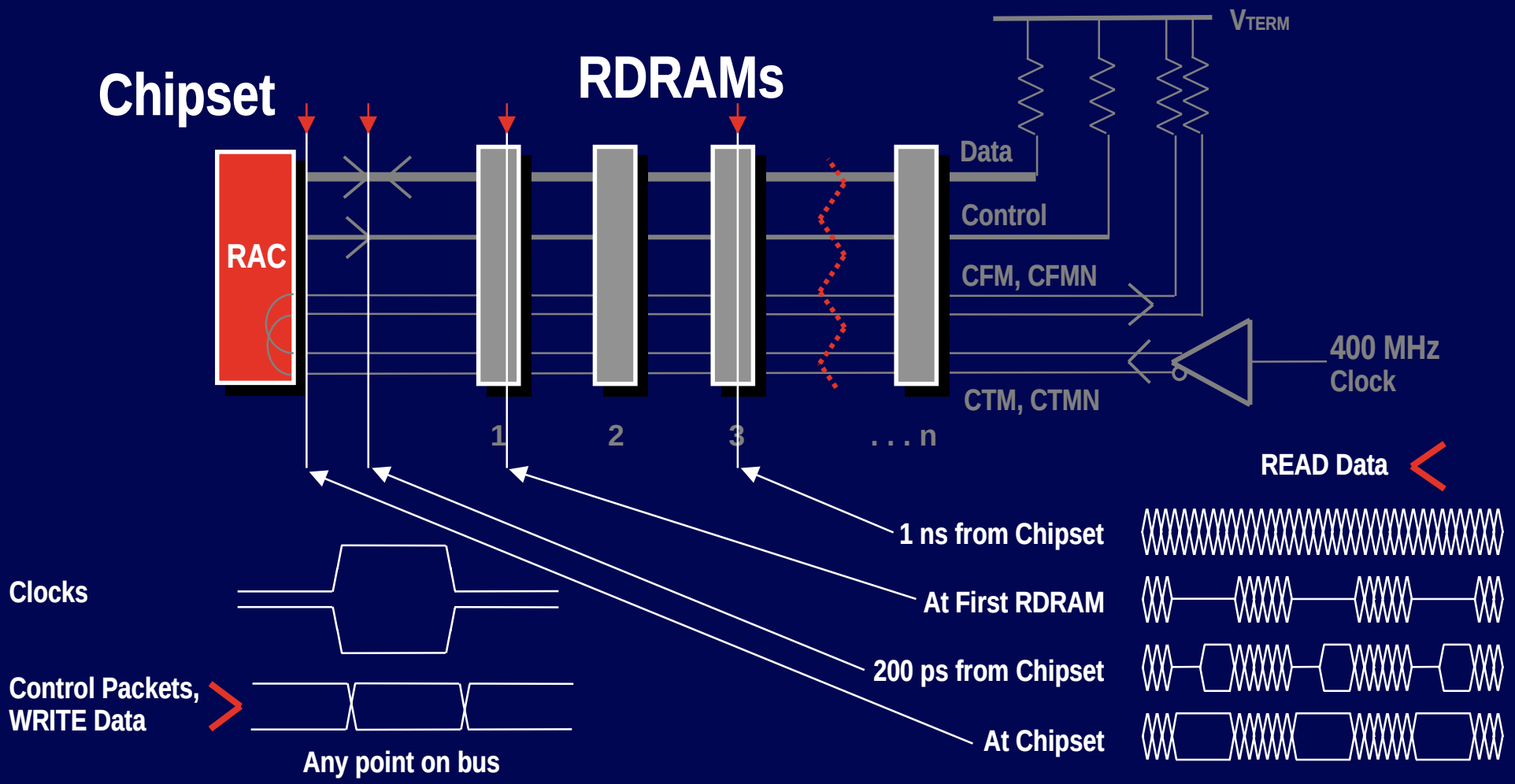
Logic Analyzer Support for Direct Rambus

- What measurement challenges does Rambus present?
- What is so unique about READ data?
- What does the Tektronix solution look like?
- How does it help?
- How do I get it?
- What related solutions does Tektronix offer?

RAMBUS® DEVELOPER

Tektronix®

Probing Rambus Direct - READ Data



RAMBUS DEVELOPER

Tektronix

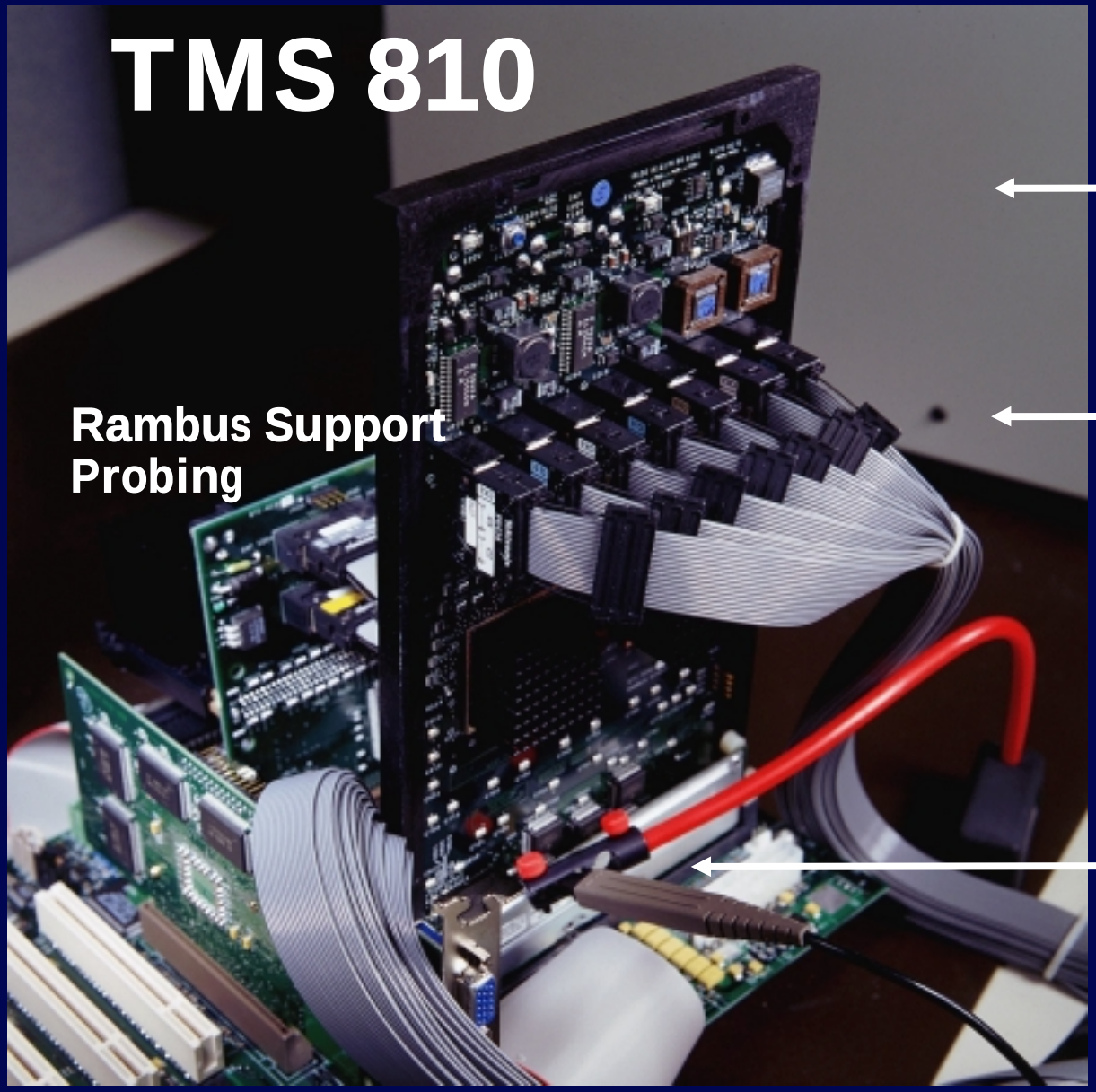
Logic Analyzer Support for Direct Rambus

- What measurement challenges does Rambus present?
- What is so unique about READ data?
- What does the Tektronix solution look like?
- How does it help?
- How do I get it?
- What related solutions does Tektronix offer?

RAMBUS® DEVELOPER

Tektronix®

TMS 810

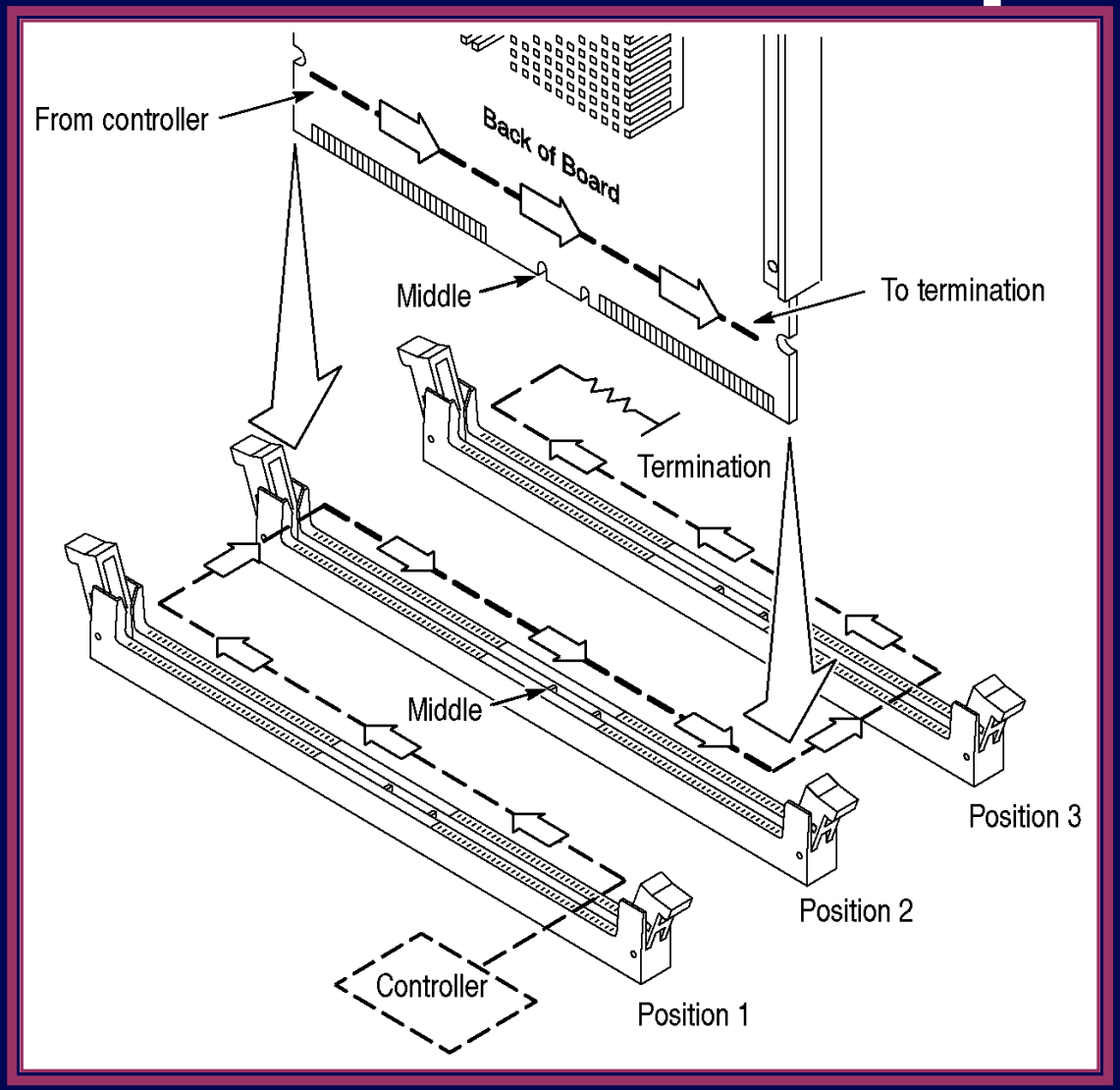


TMS 810 RIMM probe adapter

P6434 probes to logic analyzer

Fits directly into RIMM socket

RIMM Socket Probe Adapter



RAMBUS DEVELOPER

Tektronix

Rambus - Logic Analyzer Support

- Provides functional trace of bus activity
  - Synchronous acquisition at full bus speed 800 MT/S
  - Captures protocol in logical form
    - 24-bit Row control packets (3-bits wide x 8-bits deep)
    - 40-bit Column control packets (5-bits wide x 8-bits deep)
    - Packets are acquired as single parallel words
    - Packets are always aligned logically
      - Hardware barrel-shifts packets in real-time

RAMBUS® DEVELOPER

Tektronix®

Other Rambus Signals

- Rambus Serial Interface
  - Serial I/O bus
  - CMOS signals
    - SCK, Clock, max 100MHz
    - SIO0/1, 1-bit data I/O (2 pins, 1 for input, 1 for daisy-chained output)
    - CMD, 1-bit Command
  - Used at slow speed during system initialization
    - for module configuration
    - set up device addresses
  - Used at faster speed while system is operating
    - to exit Nap & PowerDown modes

Logic Analyzer Support for Direct Rambus

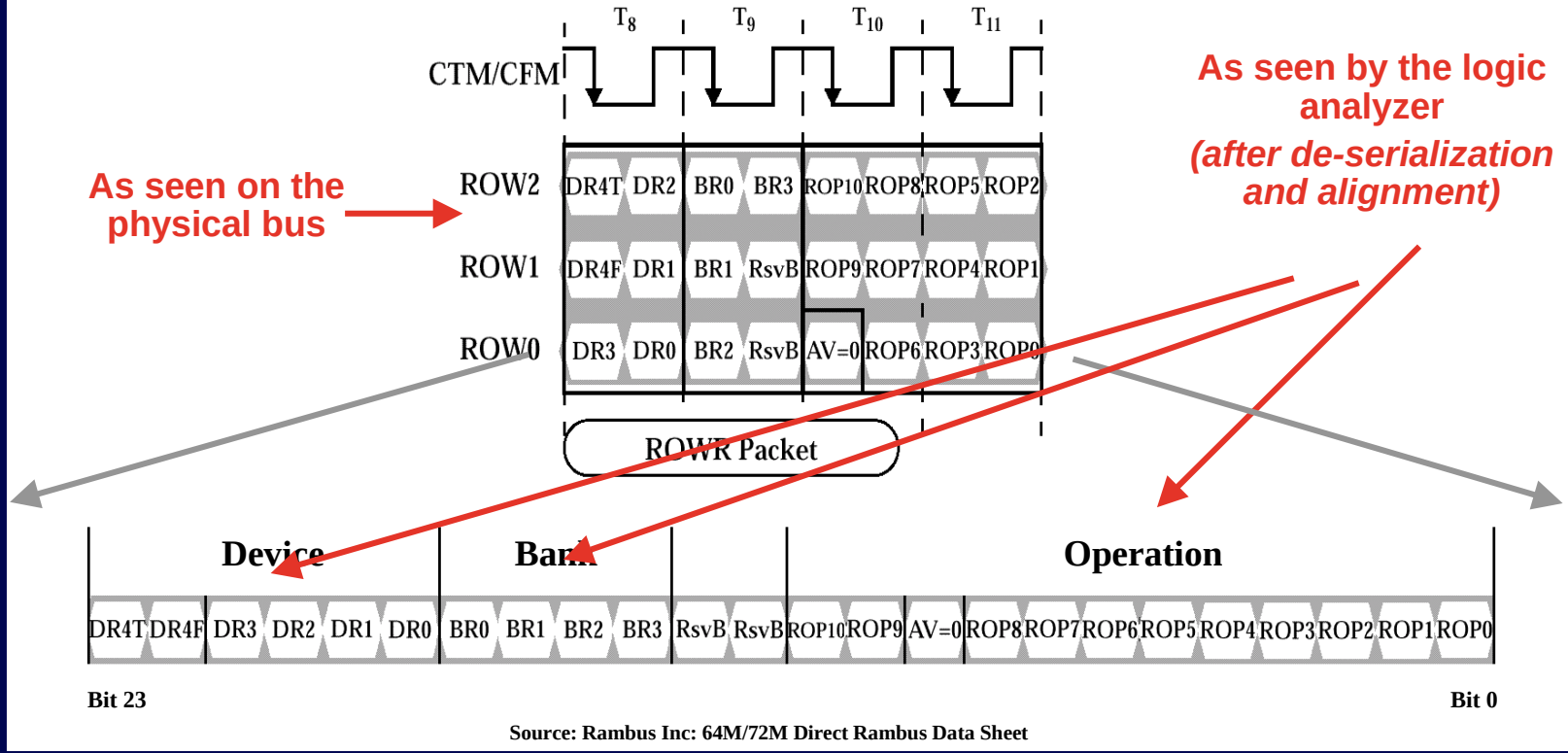
- What measurement challenges does Rambus present?
- What is so unique about READ data?
- What does the Tektronix solution look like?
- How does it help?
- How do I get it?
- What related solutions does Tektronix offer?

RAMBUS® DEVELOPER

Tektronix®

Packet De-Serialization and Alignment

EXAMPLE: ROW Packets

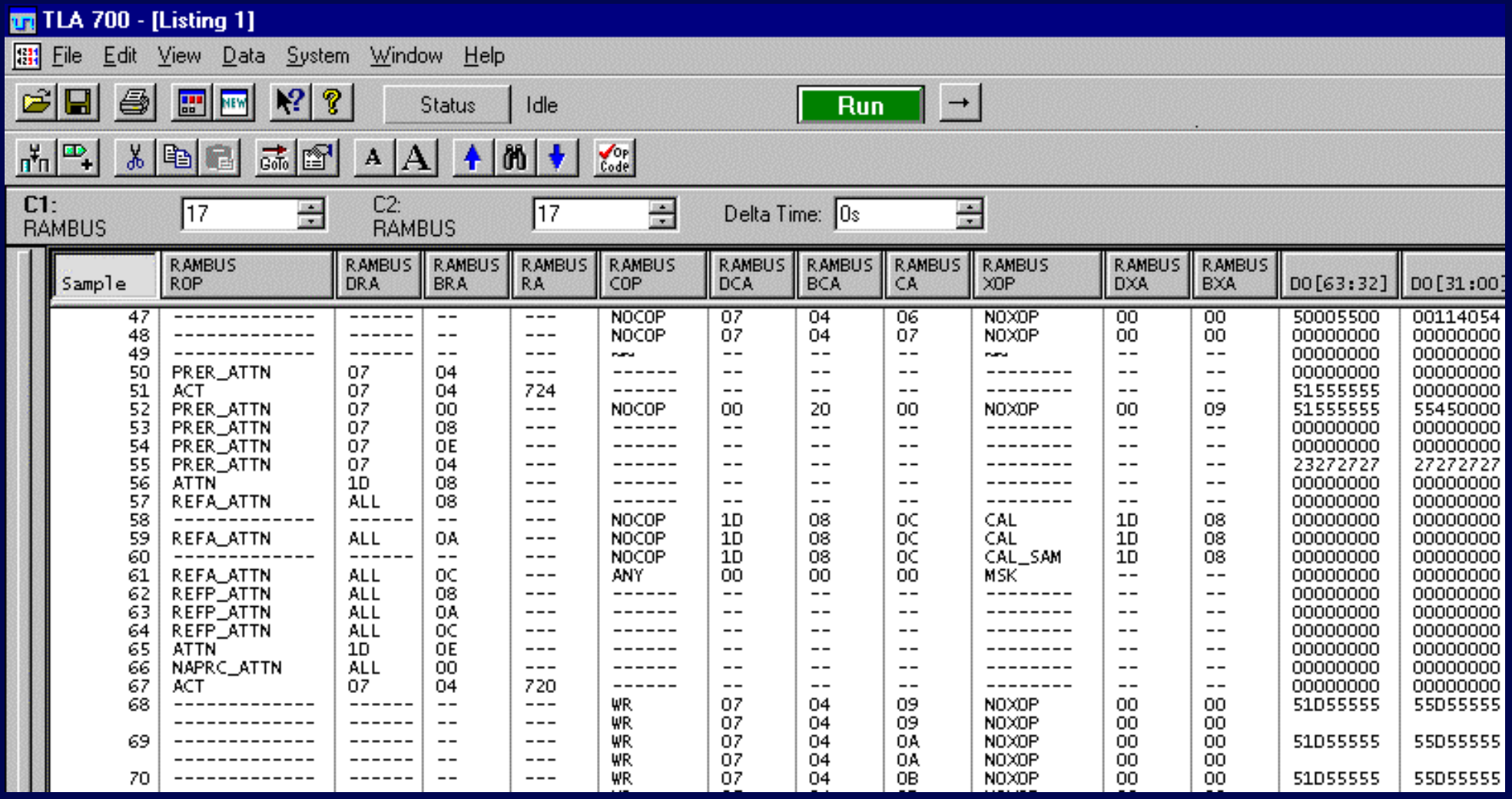


Source: Rambus Inc: 64M/72M Direct Rambus Data Sheet

RAMBUS DEVELOPER

Tektronix

Rambus Protocol Trace Display



Sample	RAMBUS ROP	RAMBUS DRA	RAMBUS BRA	RAMBUS RA	RAMBUS COP	RAMBUS DCA	RAMBUS BCA	RAMBUS CA	RAMBUS XOP	RAMBUS DXA	RAMBUS BXA	D0[63:32]	D0[31:00]
47	----------	------	--	---	NOCOP	07	04	06	NOXOP	00	00	50005500	00114054
48	----------	------	--	---	NOCOP	07	04	07	NOXOP	00	00	00000000	00000000
49	----------	------	--	---	~~	--	--	--	~~	--	--	00000000	00000000
50	PRER_ATTN	07	04	---	------	--	--	--	--------	--	--	00000000	00000000
51	ACT	07	04	724	------	--	--	--	--------	--	--	51555555	00000000
52	PRER_ATTN	07	00	---	NOCOP	00	20	00	NOXOP	00	09	51555555	55450000
53	PRER_ATTN	07	08	---	------	--	--	--	--------	--	--	00000000	00000000
54	PRER_ATTN	07	0E	---	------	--	--	--	--------	--	--	00000000	00000000
55	PRER_ATTN	07	04	---	------	--	--	--	--------	--	--	23272727	27272727
56	ATTN	1D	08	---	------	--	--	--	--------	--	--	00000000	00000000
57	REFA_ATTN	ALL	08	---	------	--	--	--	--------	--	--	00000000	00000000
58	----------	------	--	---	NOCOP	1D	08	0C	CAL	1D	08	00000000	00000000
59	REFA_ATTN	ALL	0A	---	NOCOP	1D	08	0C	CAL	1D	08	00000000	00000000
60	----------	------	--	---	NOCOP	1D	08	0C	CAL_SAM	1D	08	00000000	00000000
61	REFA_ATTN	ALL	0C	---	ANY	00	00	00	MSK	--	--	00000000	00000000
62	REFP_ATTN	ALL	08	---	------	--	--	--	--------	--	--	00000000	00000000
63	REFP_ATTN	ALL	0A	---	------	--	--	--	--------	--	--	00000000	00000000
64	REFP_ATTN	ALL	0C	---	------	--	--	--	--------	--	--	00000000	00000000
65	ATTN	1D	0E	---	------	--	--	--	--------	--	--	00000000	00000000
66	NAPRC_ATTN	ALL	00	---	------	--	--	--	--------	--	--	00000000	00000000
67	ACT	07	04	720	------	--	--	--	--------	--	--	00000000	00000000
68	----------	------	--	---	WR	07	04	09	NOXOP	00	00	51D55555	55D55555
	----------	------	--	---	WR	07	04	09	NOXOP	00	00		
69	----------	------	--	---	WR	07	04	0A	NOXOP	00	00	51D55555	55D55555
	----------	------	--	---	WR	07	04	0A	NOXOP	00	00		
70	----------	------	--	---	WR	07	04	0B	NOXOP	00	00	51D55555	55D55555

RAMBUS® DEVELOPER

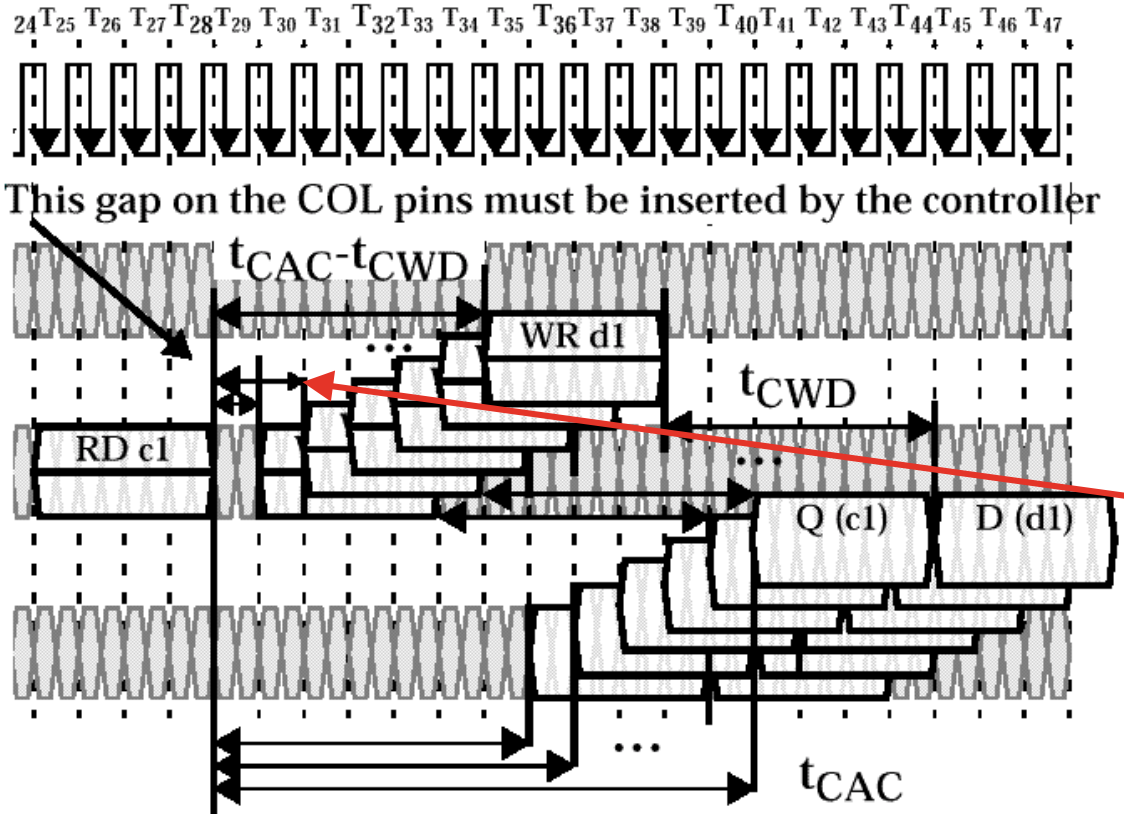
Tektronix®

Packet De-Serialization and Alignment

- De-serialized packets present protocol more logically
  - Protocol and data acquired by the logic analyzer are whole logical packets
    - Triggering is simple on single, aligned, parallel words
      - Triggering on entire Row or Column packets
      - Trigger on row followed by column
      - Simplifies and extends logic analyzer triggering capability
    - Enables symbolic trigger definition on each field of a packets
    - Enables storage qualification based on packet types
    - Trace data is much easier to understand and analyze
    - Trace depth is effectively 8 times that of the module used
    - Oscilloscopes can be easily triggered on transaction packets
      - Enables you to view signal quality at the time of specific

Packet De-Serialization and Alignment

Packet Alignment Dynamics



Packet boundary alignment varies

Source: Rambus Inc: 64M/72M Direct Rambus Data Sheet

RAMBUS DEVELOPER

Tektronix

How does it compare to other Logic Analyzer solutions for Rambus?

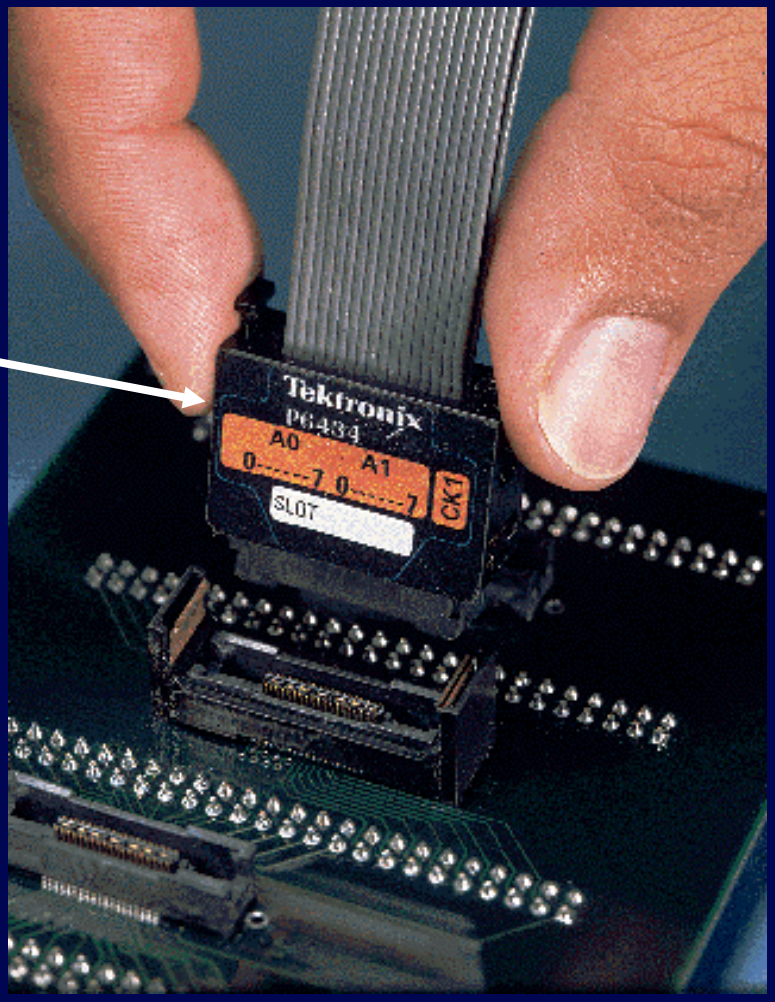
- Uses common logic analyzer modules
  - Same modules as IA32 front side bus, AGP, PCI, etc.
- Much lower system cost
- Allows useful triggering on logical protocol
  - Acquires aligned logical packets
  - 16 trigger levels
    - Can recognize entire packets in each trigger level
  - Comprehensive storage qualification
  - Trigger correlation with external 3GHz DSO

RAMBUS® DEVELOPER

Tektronix®

How does it compare to other Logic Analyzer solutions for Rambus?

- Optional depths can capture up to 265M samples of 800 MHz Rambus protocol & data
- Quick setup with seven (7) high-density Mictor probe connections
  - No individual channels to connect
- No user calibration of sample points required
- Latches data at the RIMM interface without long cables
- Supports 300-400 MHz Rambus operation



RAMBUS® DEVELOPER

Tektronix®

Triggering a DSO on Rambus Protocol

- Enables you to view signal quality of signals precisely when the bus protocol indicates you have a problem
- Requires useful & deterministic triggering on logical protocol without
- Requires a DSO with adequate bandwidth and both differential and single-ended probes
- Requires the ability to correlate the trigger points of the logic analyzer and DSO
- Is only available from Tektronix:
  - TLA 700 series logic analyzer
  - TMS 810 Rambus support
  - TDS694C 3GHz (10 GS/s) DSO

RAMBUS® DEVELOPER

Tektronix®

Logic Analyzer Support for Direct Rambus

- What measurement challenges does Rambus present?
- What does the Tektronix solution look like?
- What is so unique about READ data?
- How does it help?
- How do I get it?
- What related solutions does Tektronix offer?

RAMBUS® DEVELOPER

Tektronix®

TMS810 Rambus Support

- TLA System requirements
  - TMS 810
    - Includes RIMM probe adapter, setup and display software, manual
    - Available now
  - Requires 238 channels (a by-product of 8:1 de-serialization)
    - One 136-channel module and one 102-channel module
      - Two 136 channel modules can be used also
    - 100 MHz only (200 MHz option is not required)
    - 7 - P6434 probes
  - Memory depth
    - 64K deep modules = 512K (800 MHz) bus samples or 64K packets
    - 16M deep modules = 256M (800 MHz) bus samples or 16M packets

RAMBUS® DEVELOPER

Tektronix

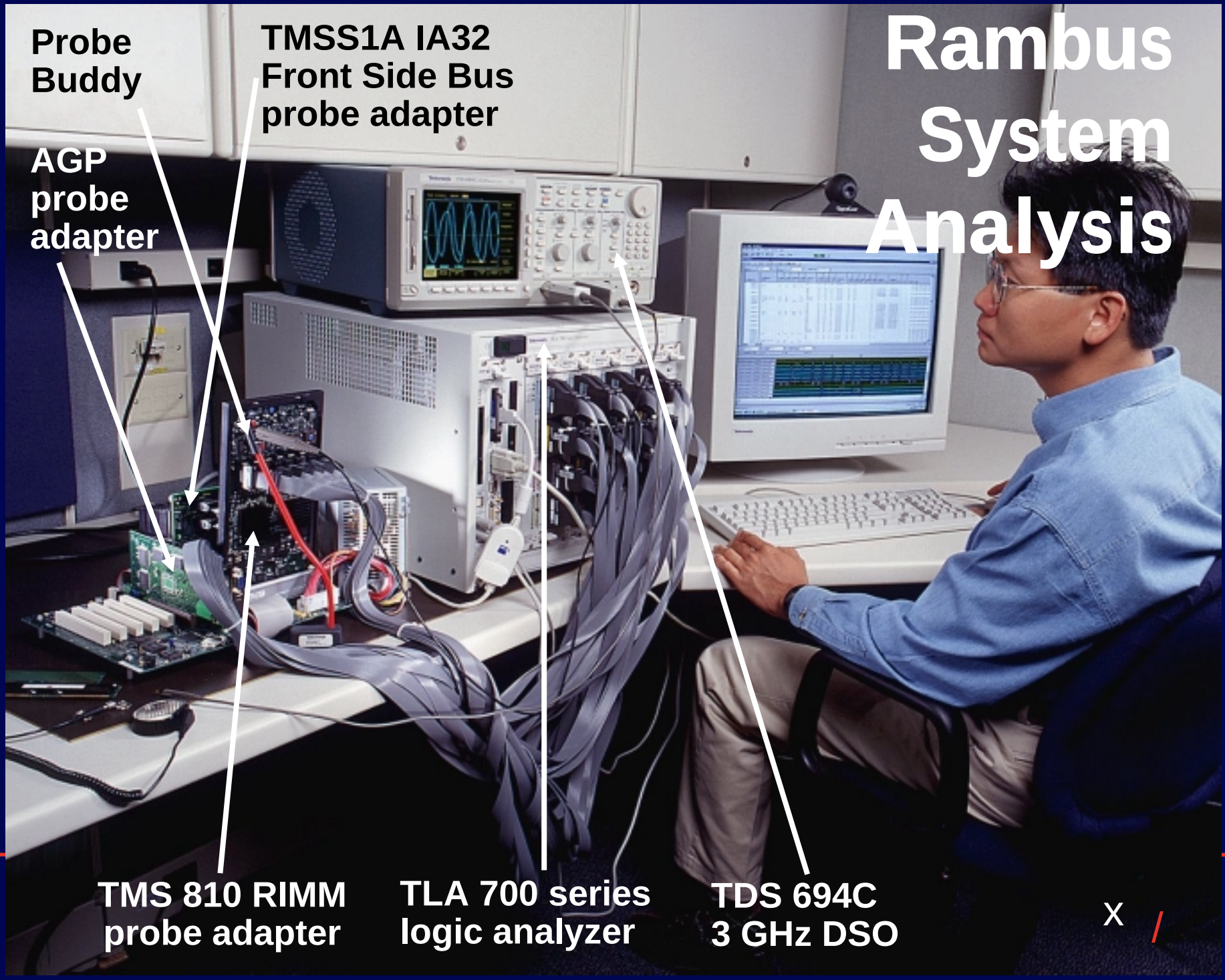
Logic Analyzer Support for Direct Rambus

- What measurement challenges does Rambus present?
- What does the Tektronix solution look like?
- What is so unique about READ data?
- How does it help?
- How do I get it?
- What related solutions does Tektronix offer?

RAMBUS® DEVELOPER

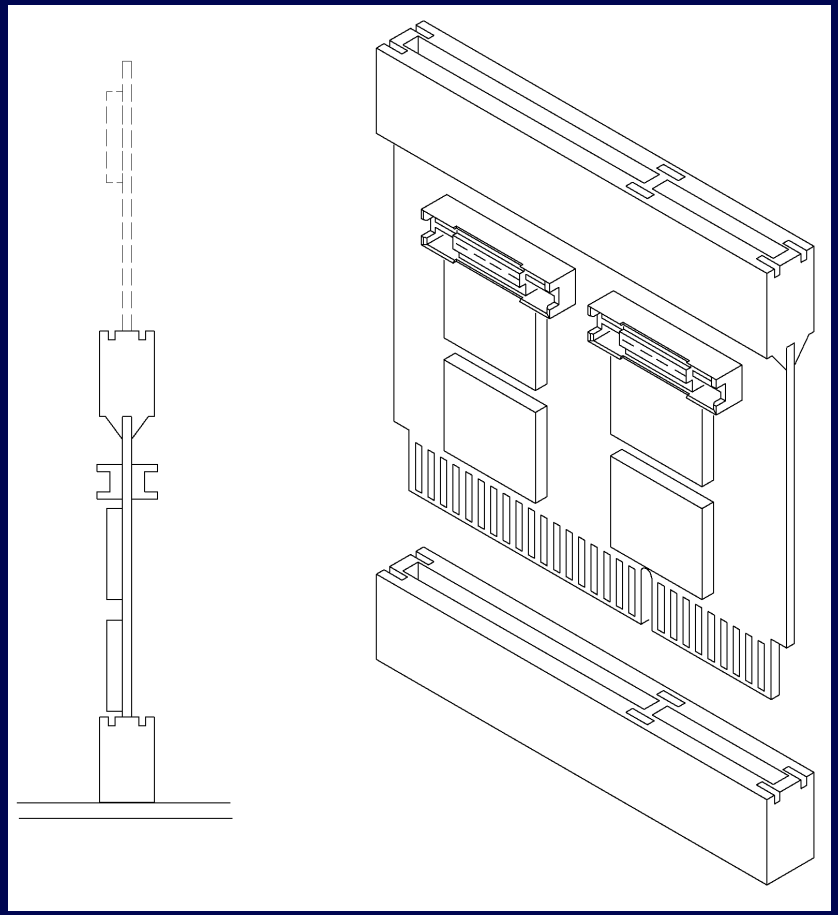
Tektronix®

Rambus System Analysis



AGP4X Support - TMS 807

- Interposer Design
- Uses Standard AGP4X connector
- Supports 1.5V Graphics Cards
- Imposes no additional bus layout constraints (length, etc.)
- Does not require calibration
- The only tool that provides accurate analysis of AGP 4x signals traveling in both directions

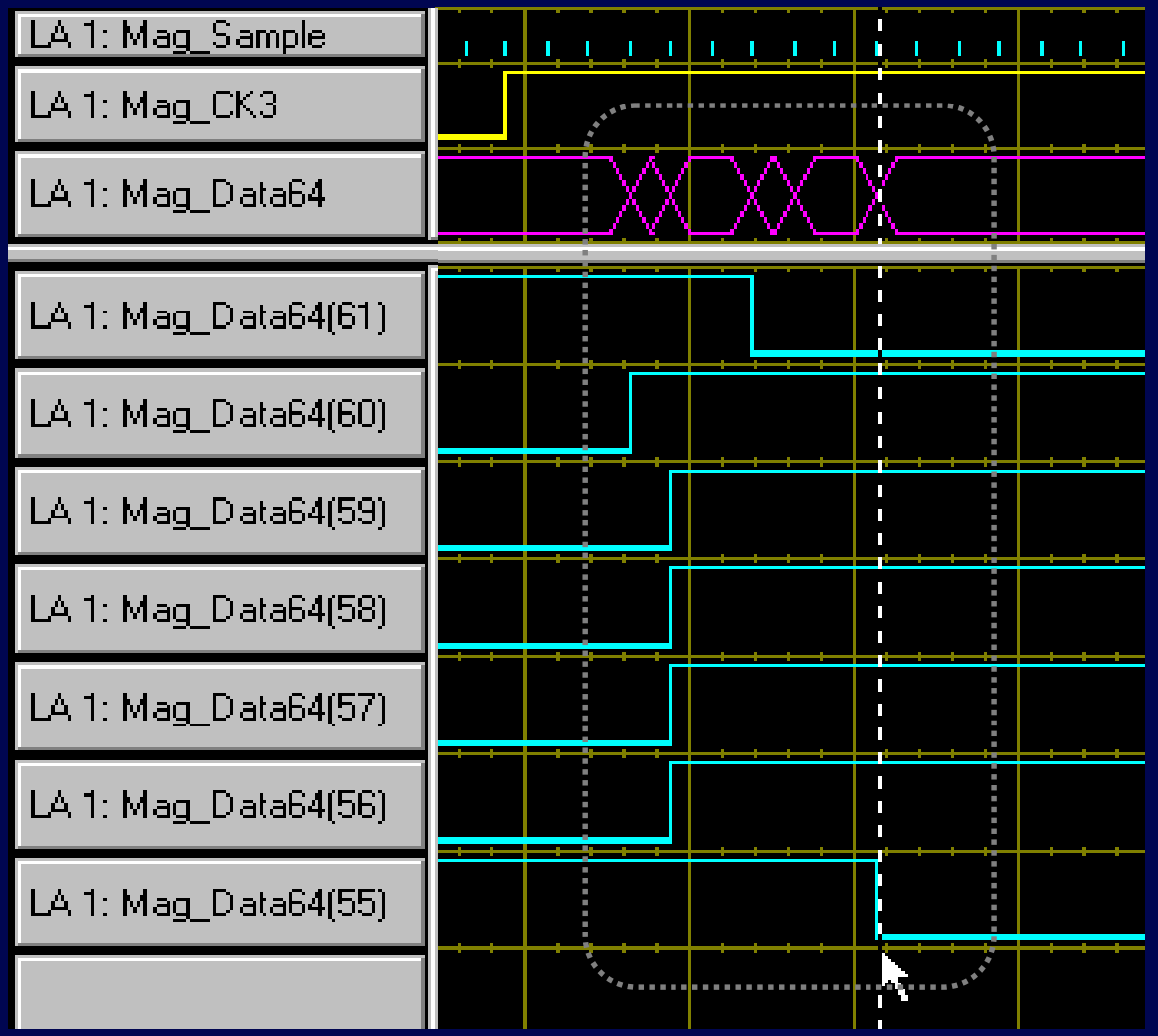


RAMBUS DEVELOPER

Tektronix

AGP4X Support - TMS 807

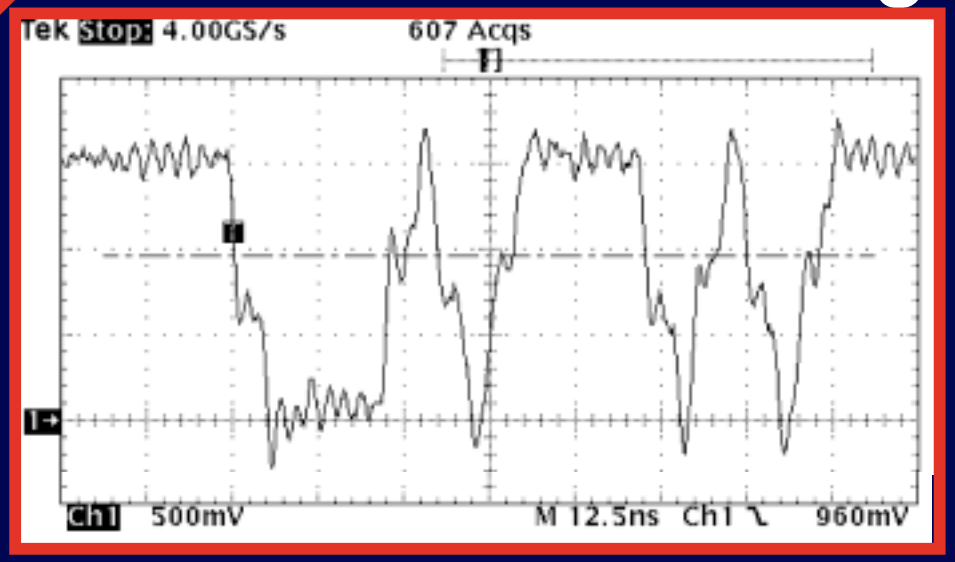
- The only tool that provides accurate timing analysis of the entire AGP 4x bus
- 2 GHz Timing analysis via MagniVu™

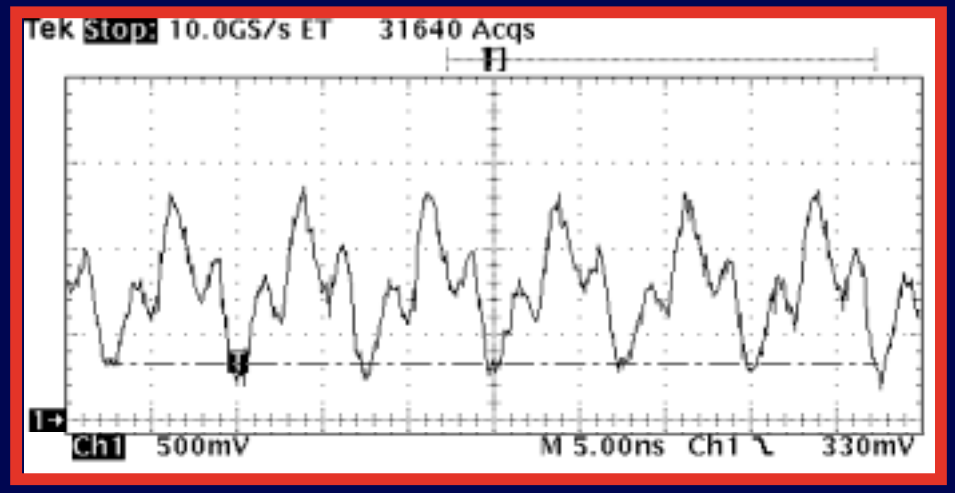


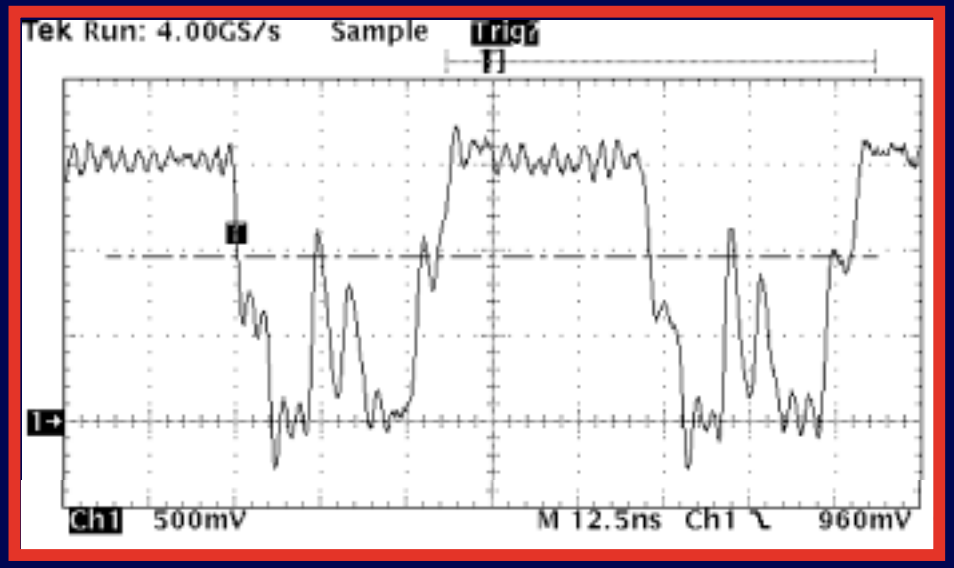
RAMBUS DEVELOPER

Tektronix

The AGP4x signal challenge





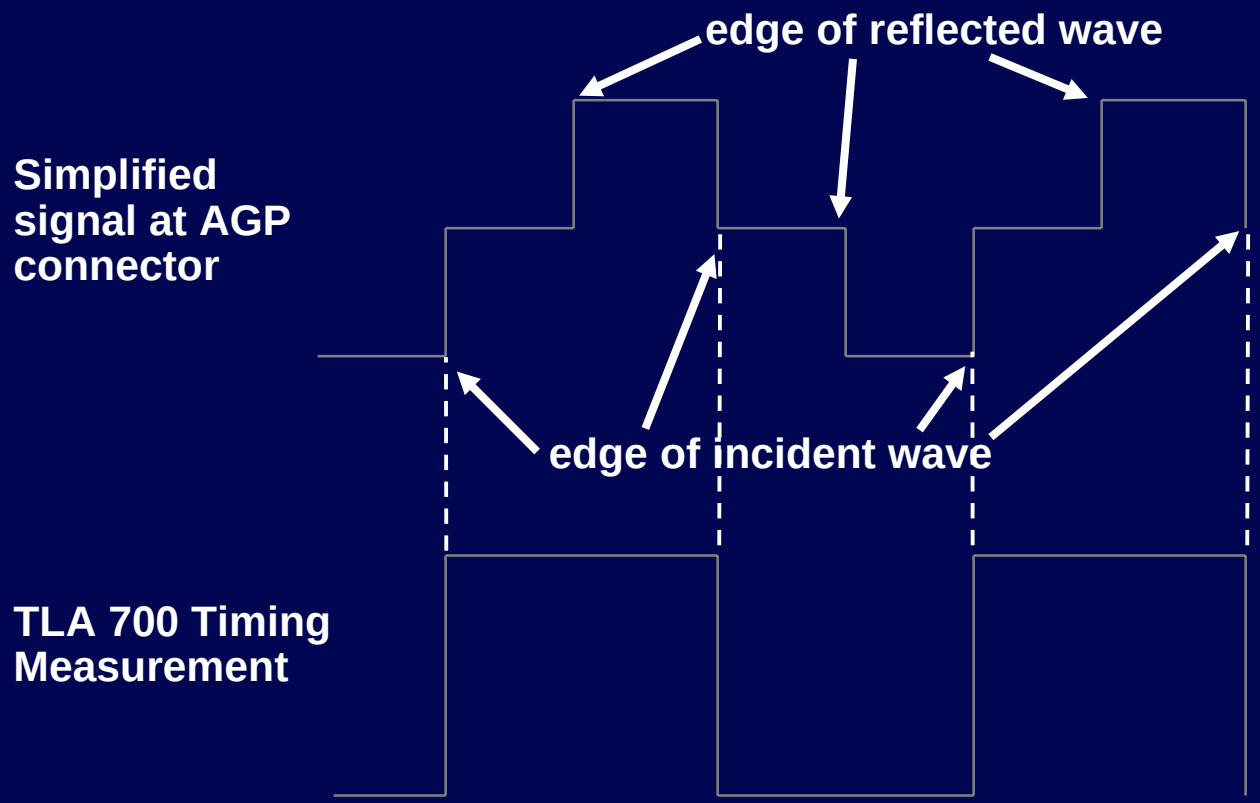


RAMBUS® DEVELOPER

Tektronix®

Analog Signal Reconstruction

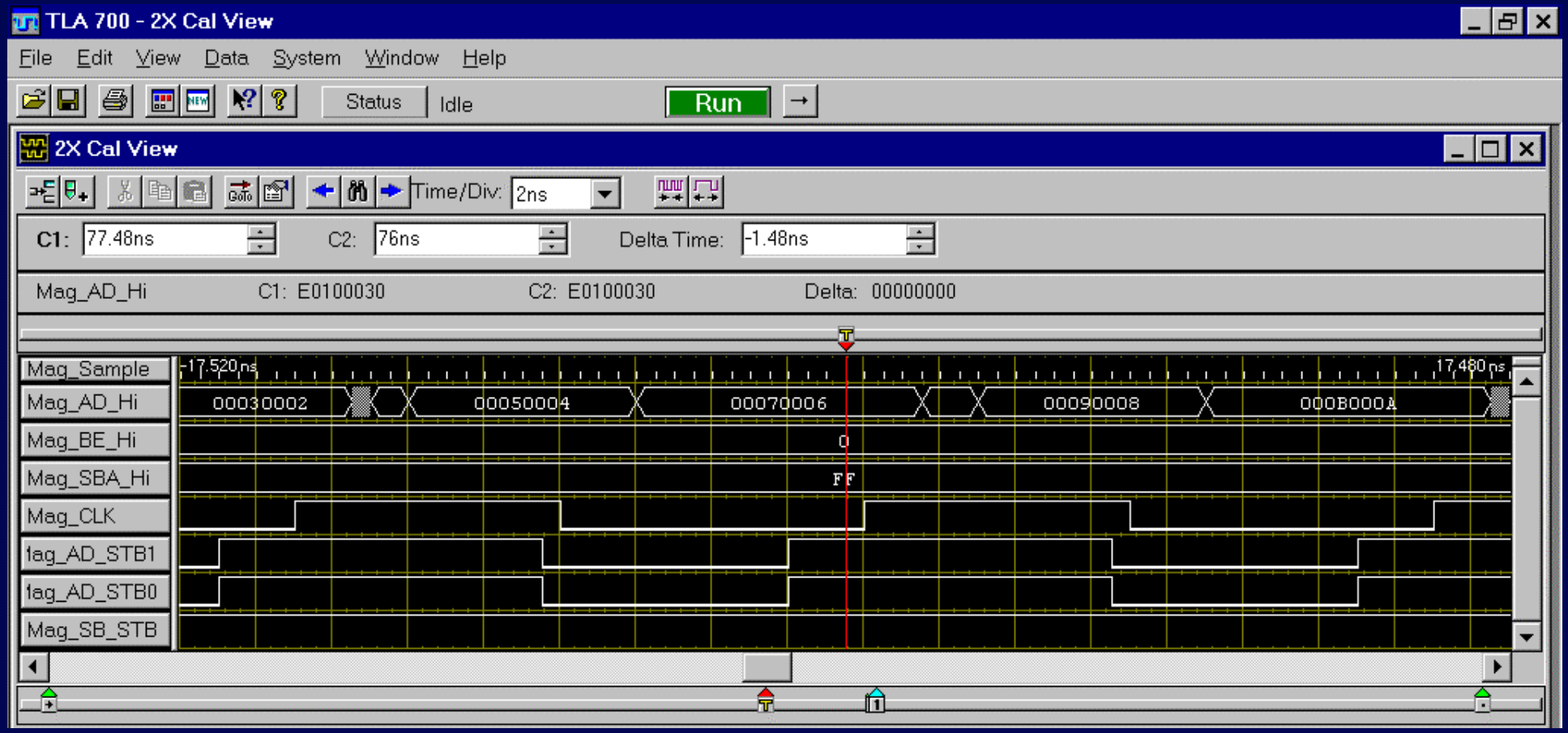
Tektronix AGP4x support reconstructs true relationship of timing edges (at the interposer)



RAMBUS DEVELOPER

Tektronix

AGP4x Timing - 500 ps Resolution



RAMBUS DEVELOPER

Tektronix

AGP4x Timing Support

Product Description

- AGP4x Timing support
- Works in all AGP modes 4x, 2x, common clock up to 133MHz

System Requirements

- (1) 102-channel LA module
- (3) P6434 High Density (Mictor) probes

Ordering Information & Pricing

- TMS 807 - $5,450

RAMBUS® DEVELOPER

Tektronix®

Other Rambus Solutions from Tektronix

- **High-bandwidth, multi-channel oscilloscopes**
- **High-bandwidth oscilloscope probes**
- **High-bandwidth differential oscilloscope probes**
- **High-resolution TDRs (Time-Domain Reflectometers)**
  - **For analyzing transmission line impedances**
- **Support for related computer and peripheral buses**
  - Pentium II/III
  - AGP 1x/2x/4x
  - PCI
  - USB
  - APIC
  - iEEE 1394
  - many more...

RAMBUS® DEVELOPER

Tektronix®